AMMAR SARWAR

Design Verification Engineer

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SUMMARY

Design Verification Engineer with hands-on experience in UVM-based environments, specializing in RISC-V and SystemVerilog. Skilled in building scalable verification frameworks for complex SoCs and IPs. Proven expertise in functional coverage, assertions, and constrained-random testing

EXPERIENCE

Verification Engineer

10xEngineers Technologies Pvt Ltd

08/2024 - Present Lahore, Pakistan

Verification of RISC-V-Based IOMMU IP for a Leading US-Based Client

- Developed a UVM-based verification environment for RISC-V IOMMU with a team of four
- Developed a comprehensive testplan for the IOMMU walk model
- Developed an IOMMU walk reference model with support for G-stage, VS-stage, SVNAPOT, MSI, and nested translation
- Implemented detection of illegal PTEs with support for Super Pages and Global Pages
- Added DV support for Writing Fault Error Record to In Memory Fault Queue and generating MSI
- Developed a memory management block to allocate memory for each transaction, supporting infinite back-to-back LTI transactions
- Developed a reusable LTI Request Generator for IOMMU and TWE levels
- Authored and reviewed the RISC-V IOMMU IP fault test plan at both system and block levels
- Writing and executing test cases for architectural, PMA, and PMP registers
- Led a 25-person team for 3+ months, ensuring seamless client coordination

Verification Engineer

10xEngineers Technologies Pvt Ltd

10/2023 - 07/2024 Pakistan

Worked as part of a 15-person team for the US-based client *DreamBig Semi*, where we designed and verified the RISC-V IOMMU IP. During my 9-month tenure, I

- Developed a comprehensive memory management model for verifying RISC-V IOMMU IP translation requests, managing memory setup for each transaction and supporting First Stage, Second Stage, Nested Translation, MSI Translation, Page Request PRI, and cache invalidation requests
- Understood the specification of the AMBA ACE5 lite, AXI5 Stream, LTI and DTI-ATS protocols
- Wrote 350+ block-level tests and 200+ system-level tests for verification
- Executed a comprehensive IOMMU fault test plan covering DTI TBU and DTI ATS and LTI transaction fault cases
- Troubleshooted third party VIPs and worked with the vendor to resolve the issues
- Added checkers for IOTLB, PCIe Translation Requests, and Fault detection in the scoreboard
- Worked with the design and verification team achieving 100% line and function coverage for comprehensive feature verification
- Served as Tech Lead for three associate engineers, successfully onboarding them to the project

EDUCATION

Bachelor of Science in Electrical and Computer Engineering

University of Engineering and Technology, Lahore

09/2019 - 03/2023 Lahore, Pakistan

KEY ACHIEVEMENTS

Gold Medal & High Achiever Award

Awarded the Gold Medal and prize money for outstanding performance at the LGES High Achiever Ceremony

Subject Matter Expert

Served as an SME for System Verilog verification and Intro to RISC-V Assembly & Computer Architecture courses, contributing to curriculum development and instruction at 10xE Training Department.

PROJECTS & OPEN-SOURCE CONTRIBUTION

AMBA-AHB3 LITE PROTOCOL

01/2023 - 02/2023 10xEngineers

Verification of AMBA AHB3 Slave Lite Protocol

- Conducted comprehensive verification of the AMBA AHB3 Slave Lite Protocol using System Verilog
- Developed a three-layered testbench comprising numerous tests to ensure thorough validation

ACTs for CVA6 (openHW Group)

07/2023 - 09/2023 10xEngineers

Contributed to architectural verification for Open HW group (*PR#1376*)

- A comprehensive test plan was executed, involving a series of self-written tests, to ensure the architectural verification of RISC-V MMU SV32
- Successfully merged into the official repository of CVA 6 Open HW group

RISCV Arch Test

11/2023 - 12/2023 10xEngineers

Architectural tests for RISC-V architecture (*PR#407*)

- Introduced a comprehensive suite of self-checking assembly tests for MMU SV39 and Sv48 verification
- Validated over 110 tests using SPIKE as the DUT and SAIL as a reference

EXPERIENCE

Associate Engineer

10xEngineers Technologies Pvt Ltd

07/2022 - 09/2023 Pakistan

Joined 10xEngineers as an Associate Engineer on July 2022

- Where I undertook coursework in computer architecture, RISC-V Assembly, System Verilog for verification, UVM, C, Python programming, basics of Linux, and Git, expanding my knowledge base and skill set

Teaching Assistant

University of Engineering and Technology, Lahore

2021 - 01/2022 Lahore, Pakistan

A prestigious institution focused on engineering and technology education

- Worked as a Teaching Assistant for the course of Programming Fundamentals & Digital System Design

SKILLS/TOOLS

UVM, SystemVerilog, SVAssertions, Constrained Random Testing,

Coverage, Hypervisor, Testplan, C/Python, GTKwave, Verdi, JIRA,

Confluence, ModelSim, QuestaSim, RISCOF, SPIKE, SAIL,

Synopsys VCS, Xilinx Vivado, Cadence, AMBA(AXI,AHB,APB),

LTI/DTI-ATS, Git/GitLab

Technical Keywords

RISC-V, Assembly, UVM, SystemVerilog, SV Assertions, Functional Coverage, Constrained Random Testing, CPU Verification, Testbench Architecture, IP/SoC Verification, RTL Design, Coverage Closure, AMBA (AXI, AHB, APB), LTI, DTI, Debugging, Regression Testing, Simulation Tools, DV Methodologies

PROJECTS & OPEN-SOURCE CONTRIBUTION

RISCOF CTG

11/2023 - 12/2023 10xEngineers

RISC-V compliance testing project (*PR#89*)

- Incorporated coverpoint definitions for assembly tests enhancing MMU SV39, Sv48 verification

Misaligned Access Support in SAIL

01/2024 - 03/2024 10xEngineers

Improvement on RISC-V reference model SAIL

- Implemented misaligned memory access support in the RISC-V reference model SAIL

RISC-V PROCESSOR with RISCOF Compliance Testing

11/2022 - 12/2022 UET

Developed the different RISC-V Processors that underwent compliance testing using the RISCOF framework

- RV32I Single Cycle Processor
- RV32I Three Staged Pipelined Processor
- RV32I Five Staged Pipelined Processor
- M Standard Extension for Integer Multiplication and Division with 5 Stage Pipelined Processor

AMBA APB AHB AXI Protocol Verification

10/2024 - 2/2025 10xEngineers

Developed reusable UVCs for AMBA AXI, AHB, and APB protocols using SystemVerilog and UVM. Designed and implemented complete verification environments with key components such as sequencer, driver, monitor, scoreboard, and responder, following standard UVM architecture. Ensured protocol compliance through functional coverage and assertions.